Claims

[c1] 1. A method to lower a demand in an alignment accuracy in an integrated circuit manufacturing process, the method comprising:
providing a substrate;
forming a first mask layer over the substrate, wherein the first mask layer comprises a plurality of first openings and at least a second opening;
filling the first openings and the second opening with a buffer layer;
forming a second mask layer over the substrate;
patterning the second mask layer to form at least a third opening, wherein the third opening exposes at least a portion of the buffer layer in the second opening;
performing isotropic etching to remove the buffer layer in the second opening; and
removing the second mask layer to expose the first mask layer, wherein the first opening in the first mask layer is filled with the buffer layer while the second opening is not filled with the buffer layer.

[c2] 2. The method of claim 1, wherein filling the first openings and the second opening with the buffer layer com-

prises:

forming a buffer material layer over the substrate to fill the first opening and the second opening and to cover the first mask layer; and

removing the buffer material layer that covers the first mask layer.

[c3] 3. The method of claim 2, wherein removing the buffer layer includes performing an etch back process.

[c4] 4. The method of claim 2, wherein removing the buffer that covers the mask layer includes performing a chemical mechanical polishing process.

[c5] 5. The method of claim 1, wherein the buffer layer is formed with a spin-on material or a metal.

[c6] 6. The method of claim 1, wherein when the buffer layer is a spin-on material, the buffer layer in the second opening is removed using a solution that comprises a hydrofluoric acid.

[c7] 7. The method of claim 1, wherein removing the buffer layer in the second opening is by wet etching.

[c8] 8. The method of claim 1, wherein the first mask layer comprises silicon oxide.

[c9] 9. The method of claim 1, wherein the second mask layer

includes a photoresist layer.

[c10] 10. The method of claim 1, wherein the first openings and the second opening form an array of openings.

[c11] 11. A method to lower an expectation in an alignment accuracy in an integrated circuit fabrication process, the method comprising:
providing a substrate;
forming an embedded layer over the substrate, wherein the embedded layer is formed by embedding a first material layer and a second material layer, wherein the first material layer is in a non-continuous phase, and the first material layer and the second material that encompasses the first material layer forms a continuous phase, and the first material layer is divided into a plurality first regions of the first material layer and at least a second region of the first material layer;
forming a mask layer over the substrate;
patterning the mask layer to form at least a first opening, wherein the first opening exposes at least the first material layer in the second region;
isotropic etching the first material layer in the second region to expose a sidewall of the second material layer that encompasses the first material layer in the second region to form a second opening; and
removing the mask layer to expose the embedded layer

that already comprises the second opening.

[c12] 12. The method of claim 11, wherein the non-continuous phase first material layer forms an array, and the first material in the second region is an element of the array.

[c13] 13. The method of claim 11, wherein forming the embedded layer includes forming a first material layer over the substrate, followed by encompassing the first material layer with the second material layer.

[c14] 14. The method of claim 11, wherein forming the embedded layer includes forming a second material layer over the substrate, following by embedding the first material layer in the second material layer.

[c15] 15. The method of claim 11, wherein the first material layer is formed with a spin-on material or a metal, and the second material is formed with a material that comprises silicon oxide.

[c16] 16. The method of claim 15, wherein the spin-on material includes spin-on glass, and the metal includes tungsten, titanium or titanium nitride.

[c17] 17. The method of claim 16, wherein when the first material layer is spin-on glass, the first material layer in the

second region is removed by a solution that comprises an hydrofluoric acid.

[c18] 18. The method of claim 11, wherein removing the first material layer in the second region includes wet etching.

[c19] 19. The method of claim 11, wherein the mask layer includes a photoresist layer.